

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY GURAJADA VIZIANAGARAM
IV B. Tech I Semester Advanced Supplementary Examinations March 2025
DIGITAL LOGIC DESIGN

(Open Elective)

Time: 3 hours

Max. Marks: 70

Answer any **FIVE** Questions **ONE** Question from **Each unit**
 All Questions Carry Equal Marks

UNIT-I

1. a) Convert the following to the corresponding bases : [7M]
 i) $(343)_5 = (\text{---})_7$ ii) $(7654)_8 = (\text{---})_{10}$

- b) Derive the product of maxterms for $f(a,b,c,d)=a.b.c+ b'.d+c.d'$. [7M]
 (OR)

2. a) Simplify the following expression using Boolean algebra rules : [7M]

$$Y = \overline{\overline{AB} + ABC + A(B + \overline{AB})}$$

- b) Derive and Implement Exclusive OR function involving three variables using only NOR function. [7M]

UNIT-II

3. a) Simplify the following Boolean function with the don't conditions d using K map method: $F(A, B, C, D)=\Sigma(1,3,8,10,15);$ [7M]
 $d(A, B, C, D)=\Sigma(0, 2, 9).$

- b) Explain the operation of a carry look ahead adder circuit with neat diagram. [7M]

(OR)

4. a) Design a full subtractor circuit using two half subtractor circuits. [7M]
 b) Construct a BCD adder circuit and explain its operation. [7M]

UNIT-III

5. a) Define decoder. Construct 3x8 decoder using logic gates and truth table. [7M]
 b) Draw the pin diagram and explain the functions of IC 74154. [7M]

(OR)

6. a) Design and implement Full adder with PLA. [7M]
 b) Draw the pin diagram and explain the functions of IC 7447. [7M]

UNIT-IV

7. a) Analyze D-latch using R-S latch? How it is different from D-flip flop. Draw the circuit using NAND gates and explain. [7M]
 b) Draw the logic diagram of a JK flip-flop and using excitation table explain its operation. [7M]

(OR)

8. a) What are the different types of registers? Explain the Parallel Input Serial Output shift register. [7M]
 b) Explain the operation of 4-stage twisted ring counter with circuit diagram and timing diagram [7M]

UNIT-V

9. a) Outline the steps involved in reducing a state table with an example to demonstrate minimization. [7M]
b) Discuss the process of analyzing a clocked sequential circuit using the state diagram and state table method. [7M]

(OR)

10. a) Distinguish between Mealy and Moore machines. [7M]
b) Convert the following Mealy machine into a corresponding Moore machine: [7M]

PS	NS,Z	
	X=0	X=1
A	B,0	E,0
B	E,0	D,0
C	D,1	A,0
D	C,1	E,0
E	B,0	D,0
